What is claimed is:

1. An on-DRAM termination resistance control circuit for adjusting a resistance within a semiconductor memory device that performs an on-DRAM termination operation, comprising:

push-up resistance adjusting means for adjusting resistances of a first and a second inner resistors based on an external reference resistor;

pull-down resistance adjusting means for adjusting a resistance of a third resistor based on the second inner resistor that is adjusted by the push-up resistance control means; and

resistance adjustment control means for controlling to alternatively repeat the operations of the push-up resistance adjusting means and the pull-down resistance adjusting means for the predetermined number of adjustment times.

2. The on-DRAM termination resistance control circuit as recited in claim 1, wherein the push-up resistance adjusting means includes:

comparing means for comparing the voltage between both ends of the external reference resistor that is coupled to the first inner resistor with a reference voltage; and

resistance adjusting means for adjusting the resistances of the first and the second inner resistors depending on the output of the comparing means, and

wherein the first and the second inner resistors vary

resistances thereof depending on the output of the resistance adjusting means.

3. The on-DRAM termination resistance control circuit as recited in claim 2, wherein the resistance adjusting means includes:

calculating means for up-counting a signal having predetermined bits by one when receiving the output of the comparing means; and

first and second push-up decoding means for adjusting the first and the second inner resistors by decoding the output of the calculating means, respectively.

4. The on-DRAM termination resistance control circuit as recited in claim 3, wherein the first and the second inner resistors are formed by a plurality of parallel coupled PMOS transistors, respectively.

5. The on-DRAM termination resistance control circuit as recited in claim 1, wherein the pull-down resistance adjusting means includes:

comparing means for comparing the voltage between both ends of the third inner resistor that is coupled to the second inner resistor with a reference voltage; and

resistance adjusting means for adjusting the resistance of the third inner resistor depending on the output of the comparing means, and

wherein the third inner resistor varies the resistance thereof depending on the output of the resistance adjusting means.

6. The on-DRAM termination resistance control circuit as recited in claim 5, wherein the resistance adjusting means includes:

calculating means for up-counting a signal having predetermined bits by one when receiving the output of the comparing means; and

pull-down decoding means for decoding the output of the calculating means to adjust the resistance of the third inner resistor

7. The on-DRAM termination resistance control circuit as recited in claim 6, wherein the third inner resistor is formed by a plurality of parallel coupled NMOS transistors.

8. The on-DRAM termination resistance control circuit of one as recited in claim 1, wherein the resistance adjustment controlling means includes:

ring oscillator controlling means for outputting a control signal to start an operation and finish the operation for the predetermined number of adjustment times depending on a resistance adjust command from external;

ring oscillator for outputting a pulse at every cycle while oscillating based on the control signal from the ring

oscillator controlling means; and

pulse counting and comparing means for counting the pulses from the ring oscillator and comparing the number of the counted pulses with the predetermined number of adjustment times to confirm equality of both numbers.

9. The on-DRAM termination resistance control circuit as recited in claim 8, wherein the ring oscillator controlling means includes:

a first PMOS transistor receiving a power-up signal as a control signal thereof, one end of the first PMOS transistor being coupled to a power voltage;

a first NMOS transistor receiving an enable input signal as a control signal thereof, coupled to the other end of the first PMOS transistor and a ground voltage;

a first inverter receiving the output of the pulse counting and comparing means as an input thereof;

a second PMOS transistor receiving the output of the first inverter as a control signal thereof, coupled to the power voltage and the other end of the first PMOS transistor;

a oppositely parallel coupled pair of a second and a third inverters coupled the other end of the first PMOS transistor ; and

a fourth and a fifth inverters, serially coupled to each other, receiving the output of the second inverter as an input thereof.

10. The on-DRAM termination resistance control circuit as recited in claim 9, wherein the ring oscillator includes:

a NOR gate receiving the output of the fourth inverter at one of two inputs thereof;

a sixth and a seventh inverters, serially coupled to each other, for buffering the output of the NOR gate;

an eighth and a ninth inverters, serially coupled to each other, for buffering the output of the seventh inverter to output to the other input of the NOR gate; and

a tenth, an eleventh and a twelfth inverters for buffering and inverting the output of the ninth inverter.

11. The on-DRAM termination resistance control circuit as recited in claim 10, wherein the pulse counting and comparing means includes:

a pulse counter for counting the pulses that are outputted from the twelfth inverter; and

adjustment times comparing means for comparing the output of the pulse counter with the predetermined number of adjustment times.

12. An on-DRAM termination resistance control method for adjusting resistance within a semiconductor memory device that performs an on-DRAM termination operation, comprising the steps of:

(a) adjusting resistances of a first and a second inner resistors based on an external reference resistor;

(b) adjusting a resistance of a third resistor based on the second inner resistor that is adjusted at the step (a); and

(c) alternatively repeating the steps (a) and (b) for a predetermined number of adjustment times.

13. The on-DRAM termination resistance control method as recited in claim 12, wherein the step (a) includes the steps of:

(d) comparing the voltage between both ends of the external reference resistor coupled to the first inner resistor with a reference voltage; and

(e) adjusting the resistances of the first and the second inner resistors depending on the comparison result of the step (d).

14. The on-DRAM termination resistance control method as recited in claim 13, wherein the step (b) includes steps of:

(f) comparing the voltage between both ends of the third inner resistor coupled to the second inner resistor with a reference voltage; and

(g) adjusting the resistance of the third inner resistor depending on the comparison result of the step (f).